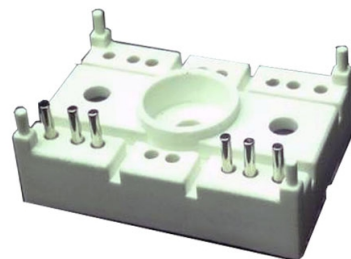


Anti-parallel Thyristor Module, 134A (Low Profile Package)

FEATURES

- High voltage
- 3000V_{RMS} isolating voltage
- High surge capability
- **Planar SCR chips**
- Heat transfer and isolation through direct copper bonded aluminum oxide ceramic (Al₂O₃ DBC)
- Simple mounting (One screw mounting)
- Compliant to RoHS
- Designed and qualified for multiple level

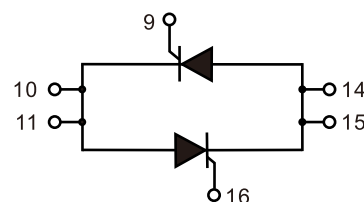


Low profile package

APPLICATIONS

- Soft starters
- Battery charges
- Light control
- Power converters
- Heat and temperature control

"KQ" Circuit Configuration :



PRODUCT SUMMARY

$I_{T(RMS)}$	134A
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MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNIT
$I_{T(RMS)}$	85°C	134	A
I_{TSM}/I_{FSM}	50 Hz	2000	
	60 Hz	2100	
I^2t	50 Hz	20	kA ² s
	60 Hz	18.3	
$I^2\sqrt{t}$		200	kA ² √s
V_{DRM}/V_{RRM}	Range	800 to 1600	V
T_J	Range	-40 to 150	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125°C mA
NK120KQ	08	800	900	15
	12	1200	1300	
	16	1600	1700	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNIT	
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave, 50Hz, $T_C = 85^{\circ}C$			134	A	
Maximum peak, one-cycle , on-state non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reappplied	Sine half wave, initial $T_J = T_J$ maximum	2000		
		t = 8.3ms			2100		
Maximum I^2t for fusing	I^2t	t = 10ms			100% V_{RRM} reappplied	20	kA^2s
		t = 8.3ms				18.3	
		t = 10ms	100% V_{RRM} reappplied		14.1		
		t = 8.3ms			12.9		
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reappplied			200	$kA^2\sqrt{s}$	
Maximum on-state voltage drop	V_{TM}	$I_{TM} = 300A$, $T_J = 25^{\circ}C$, 180° conduction			1.85	V	
Maximum holding current	I_H	Anode supply = 6V, resistive load, $T_J = 25^{\circ}C$			150	mA	
Maximum latching current	I_L				400		

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum peak reverse and off-state leakage current	I_{RRM} I_{DRM}	$T_J = 125^\circ\text{C}$	15	mA
RMS isolation Voltage	V_{ISO}	50 Hz, circuit to base, all terminals shorted	2500 (1 min) 3000 (1 s)	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67% rated V_{DRM}	1000	V/ μs

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNIT
Maximum peak gate power	P _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		10	W
Maximum average gate power	P _{G(AV)}	f = 50 Hz, T _J = T _J maximum		3	
Maximum peak gate current	I _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		3	A
Maximum peak negative gate voltage	-V _{GT}			10	V
Maximum required DC gate voltage to trigger	V _{GT}	T _J = 25°C	Anode supply = 6V, resistive load; R _a = 1Ω	0.7 to 1.5	
Maximum required DC gate current to trigger	I _{GT}			20 to 100	
Maximum gate voltage that will not trigger	V _{GD}	T _J = T _J maximum, 66.7% V _{DRM} = applied		0.25	V
Maximum gate current that will not trigger	I _{GD}			10	mA
Maximum rate of rise of turned-on current	dI/dt	T _J = 25°C, I _{GM} = 1.5A, t _r ≤0.5 μs		150	A/μs

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum junction operating temperature range	T_J		-40 to 150	°C
Maximum storage temperature range	T_{stg}		-40 to 150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.45	°C/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.18	
Mounting torque, ±10% module to heatsink, M4		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	2	N·m
Approximate weight			22	g
			0.78	oz.
Case style			Low Profile package (Nell-Top 2)	

Ordering Information Table

Device code

NK	120	KQ	12
①	②	③	④

- ① - Nell's Low profile module (Nell-Top 2)
- ② - Current rating, 120 for $I_{T(RMS)} = 134A$
- ③ - Circuit configuration type
- ④ - Voltage code x 100 = V_{DRM}/V_{RRM}

Fig.1 Forward characteristic of single thyristor

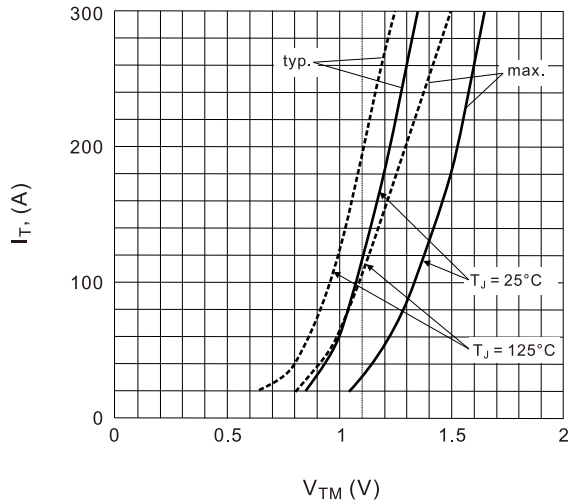


Fig.2 Transient thermal Impedance vs. time (per thyristor)

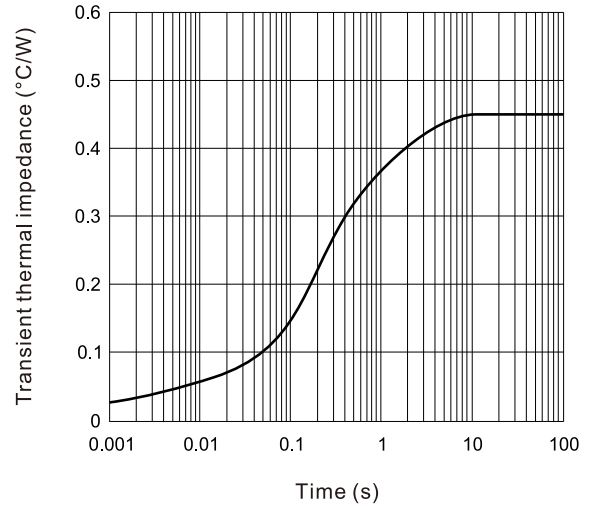


Fig.3 Power dissipation Vs. RMS current

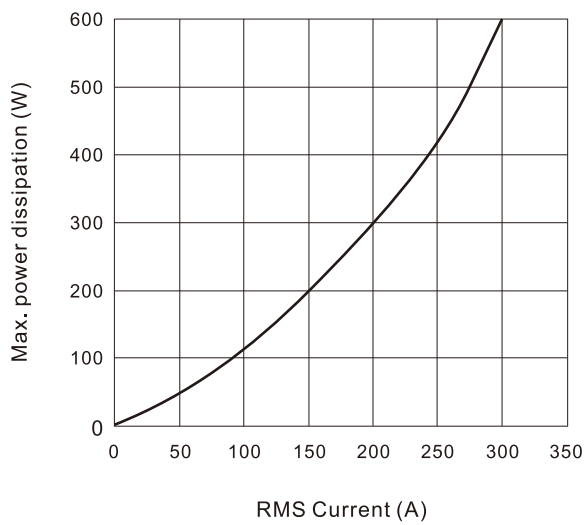


Fig.4 Surge on-state current Vs. Cycles

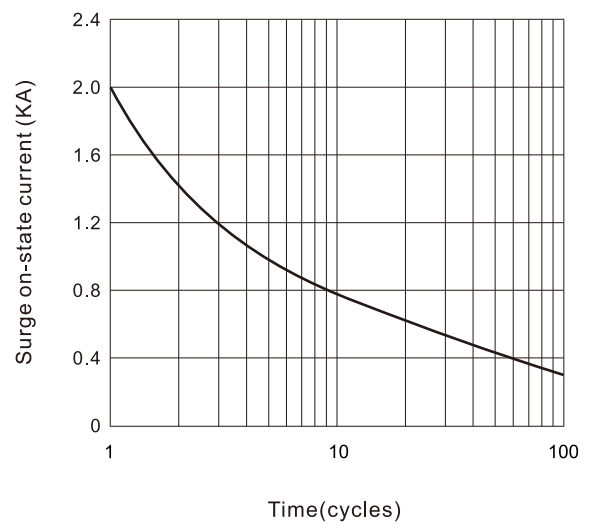
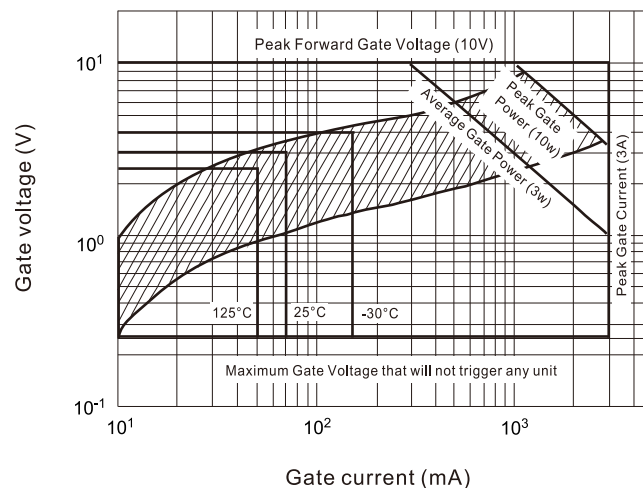
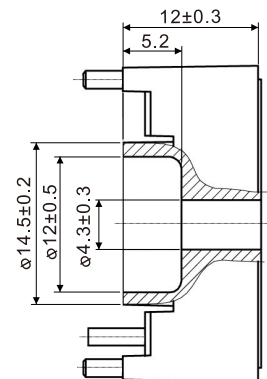
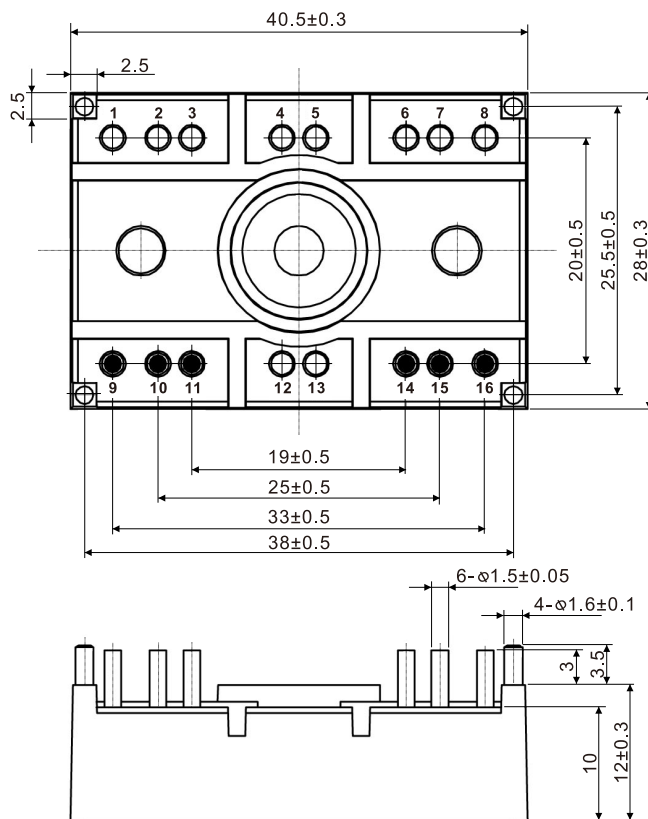
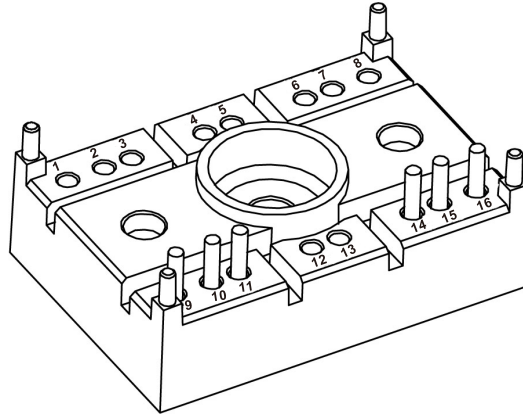
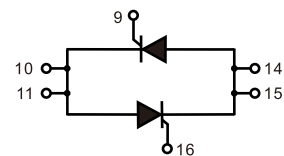


Fig.5 Gate characteristics





"KQ" Circuit Configuration :



All dimensions in millimeters(inches)